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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,118	12/22/2000	Benjamin N. Eldridge	P3D5-US	3104

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FormFactor, Inc.
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EXAMINER
ALCALA, JOSE H

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,118	ELDRIDGE ET AL.	
	Examiner	Art Unit	
	Jose H Alcala	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *60-68 and 347-361* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *60-68, 351-361* is/are rejected.

7)☒ Claim(s) *347-350* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5,8,11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 6/5/02 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because no copy of the documents is present. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 347 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear from the Specification or Drawings, how can the the second conductive and insulating layers be arranged and disposed so that outer portions of the first plurality of conductive traces are exposed. In addition it is not clear

how can the first plurality of electrical contact structures be mounted to outer portions of the first plurality of conductive traces; and a second plurality of electrical contact structures mounted to the second plurality of conductive traces.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 64-67,350 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 64, it is not clear how can the semiconductor dies be mounted to both sides of the printed circuit board, and be mounted edge-to-edge at the dame time.

Regarding Claims 65 and 66, the structural limitations of the device are not clear from the language of the claim. It is just reciting a method of making the contact structures.

Regarding Claim 350, it is not clear in lines 15-19, it is not clear if there are a third and a fourth plurality of electrical contact structures, or if it is referring to the same two plurality of conductive traces.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 60-68 rejected under 35 U.S.C. 102(b) as being anticipated by Di Stefano et al. (US Patent NO. 5,518,964).

Regarding Claim 60, Di Stefano teaches an electronic assembly (Device of figure 20), comprising: a plurality of semiconductor dies (reference number 198) mounted edge-to-edge, in close proximity to one another, on at least one side of a printed circuit board (reference number 199), each semiconductor die electrically connected to the printed circuit board by free-standing, resilient contact structures (reference number 60) mounted to each of the semiconductor dies.

Regarding Claim 61, the recitation: " that the semiconductor dies are memory devices" is an intended use limitation. it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 62, the recitation: " the electronic assembly is a single in-line memory module (SIMM)" is just a mere label for the device.

Regarding Claim 63, Di Stefano teaches that the resilient contact structures are compliant.

Regarding Claim 64,as best understood by the examinern Di Stefano teaches that the semiconductor dies are mounted to both sides of the printed circuit board. See figure 19

Regarding Claim 65, as best understood by the examiner, the limitations: " the freestanding resilient contact structures are formed by: individually bonding wires to the semiconductor dies; and overcoating the wires contemporaneously with one another" is a product by process limitation. If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even tough the prior product was made by a different process. See In re Thorpe, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding Claim 66, as best understood by the examiner, the limitations: "formed by: individually bonding wires to a sacrificial substrate; plating the wires; and gang-

transferring the plated wires to at least one of the semiconductor dies in a single step" is a product by process limitation. See explanation for claim 65.

Regarding Claim 67, the limitations: "comprising: after gang-transferring the plated wires, further plating the plated wires" is a product by process limitation. See explanation for claim 65.

Regarding Claim 68, Di Stefano teaches a ridigizing material encapsulating at least a portion of the resilient contact structure (column 9, lines 35-40)

Claims 60-68 rejected under 35 U.S.C. 102(b) as being anticipated by Di Stefano et al. (US Patent NO. 5,518,964).

8. Claims 351-361 are rejected under 35 U.S.C. 102(b) as being anticipated by Beaman et al. (US Patent No. 5,821,763).

Regarding Claim 351, Beaman teaches a semiconductor device (Figure 16), comprising: a semiconductor die (reference number 60) having a front surface (top surface) and a back (bottom surface) surface; a plurality of free-standing interconnect structures (References number 85) mounted to the front surface of the semiconductor die; and aplurality of free-standing structures mounted to the back surface of the semiconductor die (References number 42). The limitation: "heat-dissipating structures", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 352, Beaman teaches that the interconnect structures are resilient contact structures.

Regarding Claim 353, Beaman teaches that the interconnect structures are compliant contact structures.

Regarding Claim 354, Beaman teaches that the free-standing structures are wires mounted to the back surface of the semiconductor die. The limitation: "heat-dissipating structures", is an intended use limitation. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding Claim 355, Beaman teaches that the free-standing interconnect structures are of a, first material; and the free-standing heat-dissipating structures are of a second material which is different from the first material.

Regarding Claim 356, Beaman teaches that: "the free-standing interconnect structures and the free standing heat-dissipating structures are overcoated with a common material.

Regarding Claim 357, Beaman teaches : "a layer of a metallic material (reference 106) disposed between the free standing heat-dissipating structures and the back surface oft the semiconductor die, the interconnect structures are resilient contact structures.

Regarding Claim 358, Beaman teaches a semi-conductor die (Reference number 60) having a front surface (top surface) and a back surface (bottom surface); and a plurality of free-standing resilient contact structures (Reference number 85) mounted to the front surface of the semiconductor die.

Regarding Claim 359, Beaman teaches a semiconductor device (Reference number 60), further comprising: conductive pads (reference number 162) disposed on the front surface of the semiconductor die; and wherein: one contact structure is mounted to each conductive pad. See Figure 16.

Regarding Claim 360, Beaman teaches that the resilient contact structures each comprise: a wire stem (reference number 162), bonded at one end to the front surface of the semiconductor die and configured to have a springable shape; and an overcoat material applied over the wire stem and over a portion of the front surface of the semiconductor die.

Regarding Claim 361, Beaman teaches that the resilient contact structures are compliant.

Allowable Subject Matter

9. Claim 347 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Regarding Claim 347, Di Stefano teaches a semiconductor package (Device of Figure 19) comprising: first insulating layer (reference number 50); first conductive layer (reference number 38) disposed on a first surface of the first insulating layer and

patterned to have a first plurality of conductive traces (reference number 84); second insulating layer (reference number 80); second conductive layer (reference number 88) disposed on a first surface of the second insulating layer and patterned to have a second plurality of conductive traces (reference number 84) ; the first conductive layer being in contact with the second insulating layer; the second conductive and insulating layers are arranged and disposed so that outer portions of the first plurality of conductive traces are exposed (See Figure 8); a first plurality of electrical contact structures (reference number 84) mounted to outer portions of the first plurality of conductive traces; and a second plurality (another group of reference number 84) of electrical contact structures mounted to the second plurality of conductive traces. (See Figure 8)

Regarding Claim 348, Lee teaches that the first plurality of electrical contact structures extend to a plane; and the second plurality of electrical contact structures extend to the plane. (See Figure 8)

Regarding Claim 349, Lee teaches that the first plurality of electrical contact structures are resilient contact structures; and the second plurality of electrical contact structures are resilient contact structures.

Regarding Claim 350, Lee teaches that the second conductive and insulating layers are arranged and disposed so that inner portions of the first plurality of conductive traces are exposed for connecting to a semiconductor device; and further comprising: means for connecting the semiconductor device to the exposed inner portions of the first plurality of conductive traces; and means for connecting the

semiconductor device to the second plurality of conductive traces; and a first plurality of electrical contact structures mounted to outer portions of the first plurality of conductive traces; and a second plurality of electrical contact structures mounted to the second plurality of conductive traces.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
December 16, 2002

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